Optimization of the Operating Frequency of a Bidirectional Synchronous H6 Inverter

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Abstract—This paper assesses the impact of the new SiC switching technology vs. Si MOSFETs to provide optimal efficiency for a 5 kW bidirectional H6 inverter intended for residential building applications. The study applies an analytical model to predict the losses of a synchronous H6 transformer-less topology based on PSIM simulation results. The results show that SiC provides up to 98.3% efficiency compared to 93.6% achieved with Si. In addition, further improvement of efficiency is achieved by increasing the operational frequency up to 50 kHz, whereby the passive components size is also reduced.

Keywords—Bidirectional inverter, Efficiency optimization, Grid integration, High frequency, SiC MOSFET vs. Si MOSFET

IV. INTRODUCTION

DC distribution systems have received considerable attention for optimizing the efficiency of residential buildings compared to AC systems when integrated with renewable energy sources. A recent study [1] shows the potential of the DC system for reducing the loss by up to 16.5% and an increase of 3.9% in grid energy saving. However, the need for power back-up from the grid means that a bidirectional inverter is needed to maintain the DC-bus voltage under different load demand levels. It has been indicated that the average load consumption for householders is approximately 1.5 kWh (per person) in which the dominant contributions occur in winter for a climate such as Ireland. Therefore, the authors of [2] proposed a high efficiency synchronous H6 bidirectional inverter (shown in Figure 1) to overcome the impact of the light-load efficiency, in which 98.3% efficiency was achieved at 20% load using SiC semiconductors.

For more affordable applications, silicon (Si) MOSFET technologies have been utilized in transformer-less topologies for applications operated below 1 kV [3]. However, Si losses increase with increasing voltage and frequency. While SiC is more competitive in efficiency due to its lower switching loss, nevertheless, due to the fast dynamic response characteristic of SiC there are some challenges such as voltage overshoot, and the interaction between parasitic inductance and capacitance of the MOSFET body diode [4]. Mitigation of these issues has been demonstrated by considering the required damping resistor of the SiC gate [5]. A further limitation is its much higher cost than Si. The relative improvement in performance provided by SiC versus Si in a high efficiency bidirectional grid inverter is investigated in this paper so that a more informed cost-benefit analysis can be completed for different applications.

Given the high performance of SiC, it is expected that a high operational frequency might contribute to improving the performance and reducing the size and cost of passive components in a bidirectional converter. Therefore, this paper presents a framework for exploring optimization of the operating frequency of the proposed synchronous bidirectional inverter to enhance its performance in a DC distribution system. As a benchmark, the performance is compared with a Si implementation of the same converter, where Si is most widely used in bidirectional inverters for building applications [3].

Figure 1: Synchronous bidirectional inverter topology.

V. SiC VS. Si SYNCHRONOUS H6 ANALYSIS

This work is based on simulation of the novel synchronous H6 topology [2] using PSIM software with detailed analytic equations applied to predict component losses for the two different switching devices: SiC and Si, aiming to enhance the overall efficiency of the bidirectional inverter. The possibility of leveraging further off currently implemented parameters by increasing the operational frequency of the synchronous H6 is also explored.
A. Selected Semiconductor Devices

A DC operating voltage of 380 Vdc is used to compare two operational frequencies of the synchronous H6, and the grid voltage and frequency of 220 Vac and 50 Hz respectively are assumed for the AC side. The semiconductors chosen as the most suitable for the given operating conditions at a maximum power rating of 5 kW and including two switching frequencies, Fsw, of 20 kHz and 50 kHz are listed in Table 1.

TABLE I: COMPONENTS OF THE SYNCHRONOUS H6 TOPOLOGY WITH OPERATION FREQUENCY AT 20 KHZ AND 50 KHZ.

<table>
<thead>
<tr>
<th>Components</th>
<th>Model No.</th>
<th>Rated Voltage (V)</th>
<th>Rated Current (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiC MOSFET</td>
<td>C3M0120090JD</td>
<td>900</td>
<td>23</td>
</tr>
<tr>
<td>Si MOSFET</td>
<td>CVFD20065A</td>
<td>800</td>
<td>24</td>
</tr>
<tr>
<td>Inductor type</td>
<td>MPP 0055617A2</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Capacitor type</td>
<td>Film C4AF</td>
<td>250</td>
<td>16.6</td>
</tr>
</tbody>
</table>

B. Inductor Design

With increasing frequency, the filter inductance decreases by the same factor according to:

\[ L = \frac{V_{dc}}{4Fs \Delta L_{out}} \] (1)

where \( L \) is the required inductor to minimize noise caused by the switching frequency \( Fs \) for a synchronous H6 in which the maximum voltage and current under inversion and rectification were considered.

To determine the core size the following equation is applied:

\[ Core_{size} = L \cdot T^2 \] (2)

Using the core size from Eq. 2 the next step is to select the permeability of the chosen core material according to data provided by [6]. The selection criteria are based on small core size for application with a DC bias, and low core loss when operated at a low-level of AC current relative to DC current. Then, the required number of turn can be obtained from Eq. 3.

\[ N = \sqrt{\frac{L \cdot 10^3}{A_i}} \] (3)

where \( N \) represents the number of turns and \( A_i \) is inductor factor of the selected core. Finally, the maximum magnetic field intensity is calculated to ensure that the core does not saturate using Eq. 4.

\[ H = \frac{NI}{L_e} \] (4)

where \( L_e \) is the core magnetic path length, and the result determines an initial permeability from the curve fitting of permeability vs. DC bias which is illustrated in the datasheet of selected core. Iteration can be performed until a satisfactory number of turns is obtained in which the optimal inductor value can be adjusted to handle the performance.

The inductor equivalent series resistance can be calculated as follows

\[ L_{resi} = N \cdot R_{wire} \] (6)

where \( R_{wire} \) is the specified resistance of the inductor AWG wire per turn, which is selected based on its maximum current handling capacity. The total wire length is based on the core dimensions.

C. Loss Calculation

Standard equations were applied for calculating the MOSFET and inductor losses based on the circuit operating waveforms simulated in PSIM, similar to the method described in [2].

Conduction loss of the SiC MOSFETs (Pcm), MOSFET body-diodes, (Pc.eqd) and diodes (Pcd) are given as:

\[ Pcm = R_{ds,on} \cdot I_{rms,s}^2 \] (7)
\[ Pcd = V_{Fsd} \cdot I_{av,d} + R_{ds,on} \cdot I_{rms,d}^2 \] (8)
\[ P_{c_eqd} = V_{Fsm} \cdot I_{av,md} + R_{ds,on} \cdot I_{rms,md}^2 \] (9)

respectively, where Rdson_x is on resistance of the given component, while Irrmx_x is its rms current, Vfssx is the given diode component forward voltage drop and Iav_x is its average current. Switching loss of SiC MOSFETs (Psw_onm, Psw_offm) and diodes (Psw_ond, Psw_offd) are given as:

\[ P_{sw_{on,m}} = \left(V_{pkm,on} \cdot I_{pkm,on} \cdot \frac{Tr}{2} + Q_{rr} \cdot V_{pkm,on}\right) \cdot F_{sw} \] (10)
\[ P_{sw_{off,m}} = \left(V_{pkm,off} \cdot I_{pkm,off} \cdot \frac{Tf}{2}\right) \cdot F_{sw} \] (11)
\[ P_{sw_{on,d}} = \frac{1}{4} \left(V_{pkd,off} \cdot Q_{rr}\right) \cdot F_{sw} \] (12)

where, \( Tr \) & \( Tf \) are rise and fall time the MOSFETs during switching, \( Q_{rr} \) is a reverse recovery charge of the given diode, \( V_f \) and \( I_f \) are diode forward voltage and current, whereas, \( F_{sw} \) is the carrier switching frequency. Finally, MOSFET gate charge losses in (13) are given in terms of high & low side electric charge, Q, and capacitance, C, values as provided in the MOSFET datasheet:

\[ Pg = \left((Q_{g-h} \cdot Q_{g-i}) \cdot V_{gs} \cdot F_{sw}\right) + \left((C_{g-h} \cdot C_{g-i}) \cdot V_{gs}^2 \cdot F_{sw}\right) \] (13)

Using PSIM simulation, representative values of peak, average and rms voltages and currents were measured for each semiconductor component at four different time samples of each half cycle, and these were applied in (7-13) to calculate the circuit loss breakdown for different power levels.

Copper and core losses, (Pcopper, Pc) in the filter inductors were calculated according to:

\[ Pcopper = I_{rms}^2 \cdot R_{wire} \] (14)
\[ P_{\text{core}} = \frac{P_L A_e L_e}{1000} \]  
\[ P_L = 31.32 \Delta\beta^{1.585} 20^{1.37} \]

where \( A_e \) is the cross-section area of the core, \( L_e \) its path length and \( P_L \) is core loss density as a function of AC flux \( \Delta\beta \), frequency (kHz) and the given material constants. The equivalent series resistance (ESR) loss of the capacitor is given as

\[ P_{\text{ca}} = I_{\text{rms}}^2 \text{ESR} \]

VI. RESULTS AND DISCUSSION

A. Simulation Results

The performance of the synchronous H6 topology with the implementation of SiC vs. Si MOSFET operated at two frequencies 20 kHz and 50 kHz is illustrated in this section. Loss calculations are based on the operating current and voltage waveforms for all switches, which are shown for inversion and rectification modes at 20 kHz over a complete cycle of the mains in Figure 2. Also, the inductor current waveforms are shown.

Almost the same waveforms are found for the switches and inductors when operated in rectifier mode (see Figure 2 (c) and (d)). Operation at 50 kHz is found to have relatively similar waveforms, including for the inductor due to the the design according to (1) in section II which maintains its current ripple level. The switching waveforms of S1 and S2 are the mirror of S4 and S3 respectively. Similarly, the switching waveforms of S5&S7 corresponding to the switches waveforms of S6&S8.

To illustrate the current waveforms in each switch more clearly (according to the operation of the synchronous H6 topology as described in [2]), zoomed in current waveforms are shown for each of the circuit switches at the peak current level in Figure 3.
It is worth mentioning at this stage that the main difference between Si and SiC is due to a higher on resistance and a more significant contribution of the MOSFET body-diode in Si, both of which contribute additional conduction loss. Furthermore, while increasing the frequency reduces the inductor loss, it leads to a relatively higher semiconductor switching loss, particularly related to the off-state. This is due to the need for dissipating energy stored in the MOSFET body-diode during turn-on. Therefore there is a trade-off between semiconductor and inductor losses with increasing frequency which is shown in more detail in section III.B.

B. Loss Breakdown

A comparison of the loss breakdown for a 5 kW bidirectional synchronous H6 inverter with the implementation of Si (Rdson = 0.4 Ω) and SiC (Rdson = 0.12 Ω, see Table I) respectively at two frequencies: 20 kHz and 50 kHz, is presented in this section. At both frequencies, the results show a significant contribution of Si conduction loss at the higher power levels. In addition, the switching ON loss of the Si MOSFET is higher than SiC by up to 85% at 20% load where it is the dominant loss.
This dominant loss in Si is increased further when the frequency is increased to 50 kHz, so that the advantage of SiC becomes more evident. However, SiC also has increased switching loss but the conduction loss remains almost the same and higher frequency also results in miniaturization of the inductor with up to 65% associated inductor loss reduction. Therefore, the overall improvement in efficiency achieved by increasing the frequency is quite limited for SiC at full load, and efficiency is reduced at light load.

![Figure 4: Comparison of power loss breakdown between SiC vs. Si MOSFETs in inversion mode operated at 20 kHz and 50 kHz at; (a) 1 kW, (b) 2.5 kW, 4 kW and 5 kW.](image)

![Figure 5: Comparison of power loss breakdown between SiC vs. Si MOSFETs in rectification mode operated at 20 kHz and 50 kHz at; (a) 1 kW, (b) 2.5 kW, 4 kW and 5 kW.](image)

Similarly, in rectifier mode, while the full load losses are relatively higher than inverter mode, a significant improvement is found by employing SiC over Si, especially under light-load conditions as shown in Figure 5. It is found that the major drawback of Si is the reverse recovery effect which has an impact on the synchronous H6 topology when a freewheeling path is employed to maintain the inductor current during off state operation. In addition, the conduction loss is affected due to the characteristic of the reverse recovery charge which exists in the Si body diode. Again, it is noticed that the performance of Si tends to decrease more significantly at high operational frequency than SiC due to the impact of high switching loss along with the body-diode effect enabled during the rectification mode.

### C. Efficiency Comparison of Si vs. SiC

A comparison of the efficiency of SiC vs. Si operating in the proposed synchronous H6 topology is presented in Figure 6. The improved efficiency provided by the SiC compared to Si tends...
to be by far most significant when the operational power is reduced towards light-load. As shown in the results of loss breakdown above, this is largely due to switches conduction loss under all power level, in addition to the switching ON when operated under light load condition.

Figure 6: Efficiency comparison of SiC and Si MOSFET operated at 20k & 50k Hz in; (a) inverter mode and (b) rectification mode.

IV. CONCLUSION

In conclusion, the efficiency of a bidirectional synchronous H6 inverter suitable for application in a residential DC distribution system can be improved by employing SiC over Si MOSFETs, with particular improvement achieved at light load. A SiC MOSFET topology provides a predicted increase in efficiency up to 98.3% vs. 93.6% in comparison to Si MOSFET for loads under 20%. The improvement is due to contribution of lower SiC MOSFET conduction and inductor loss under different load conditions. However, while the inductor size is reduced, there is a decrease in overall efficiency provided by increased frequency at light load with a slight improvement at full load.

For Si, the findings have highlighted the impact of the reverse recovery effect in the synchronous H6 and illustrates the scope for addressing it by using SiC. However, it should be noted that the cost of SiC is approximately 2 times higher than Si for the same voltage and current ratings, and therefore the reduction in losses provided by the higher efficiency needs to be high enough to offset this increased cost. Work is ongoing to demonstrate the comparative performance through experimental validation. Moreover, to address the high switching loss for the Si solution, diode emulation will be considered so that it operates in a manner equivalent to the standard H6 under light-load.

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